RELEASED

RFuW Engineering Pte. Ltd.

RFD3T5N200-703

SP3T PIN Switch Driver – Positive & Negative Voltage Driver

Features:

- Supports High Output Drive Voltage and Current
- Support RFuW Engineering SP3T High Power Switches
- Operates from +5V and -15V to -200V
- Independent TTL Input Controls
- Complimentary Driver Outputs
- RoHS Compliant

Description:

The RFD3T5N200-703 surface mount PIN Switch Driver supports high biasing voltages required when operating PIN diodes switches under high power applications. The fundamental building block consists of a PIN Diode and it is the intrinsic layer which gives this device its unique characteristics. When charge is injected into the intrinsic layer it becomes highly conductive and when charge is depleted from the intrinsic layer it becomes nonconductive. As the operating power increase or the frequency of interest drops into the HF & VHF realms, the necessary biasing voltages climb into the hundreds of voltage which exceeds the capabilities of all MMIC style Switch Drivers.

This RFD3T5N200-703 has been designed to support optimum biasing voltages required to support SP3T switches operating at high power and low frequencies. It offers both positive and negative biasing voltages. The RFD3T5N200-703 operates with a positive bias voltage of +5V and a negative voltage between -15V to -200V depending on the application's power handling and frequency of operation.

The RFD3T5N200-703 driver can source up to -100mA from the negative source and up to +50mA from the +5V supply. The driver is controlled via an independent TTL control signals. There are three complimentary outputs to support the typical series-shunt PIN diode switch topology.

The RFD3T5N200-703 is packaged in a 33mm x 33mm x 8.4mm surface mount package. The device is compatible with surface mount, solder reflow processes typically employed in high volume production.

Environmental Capabilities

The RFD3T5N200-703 Driver is capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

ESD and Moisture Sensitivity Rating

The ESD rating for this device is Class 1A, HBM. The moisture sensitivity level rating is MSL1.

Absolute Maximum Ratings

T_A= +25ºC as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Input Voltage, $+V_{CC}$		-0.1 to 5.5 V
Input Voltage, $-V_{EE}$		0.1 to -210 V
Control Port Input Voltage		-0.5 to 5.5 V
$-V_{EE}$ Output Sink Current	V_{OUT} ~ $-V_{EE}$ V	-125 mA
$+V_{CC}$ Output Source Current	V_{OUT} ~ $+V_{CC}$ V	+60 mA
Operating Temperature		-40ºC to 85ºC
Storage Temperature		-65ºC to 150ºC
Assembly Temperature	T < 10 sec	+260ºC
Total Dissipated Power	T_{CASE} = 85ºC	6.0 W

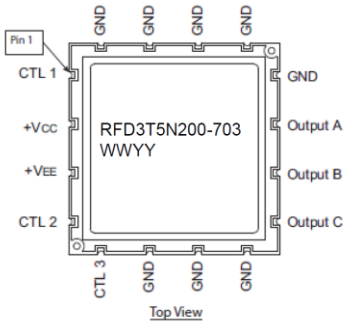
Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

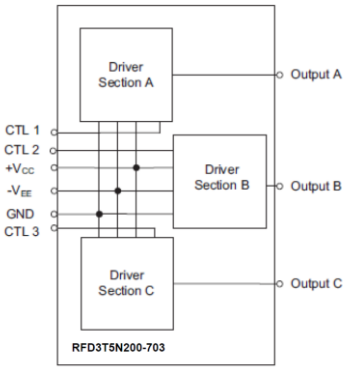
RFD3T5N200-703 Electrical Specifications

@ Z_o=50Ω, TA= +25ºC as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Operating Frequency	PRF		0	100	500	KHz
Supply Voltage	$+V_{CC}$		4.5	5	5.5	V
Supply Voltage	$-V_{EE}$		-15	-50	-200	dB/ºC
Quiescent Current ($+V_{CC}$)	I_{Q1}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, No load connected to output A & B	10	20	30	mA
Quiescent Current (=V_{EE})	I_{Q2}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, No load connected to output A & B	-15	-25	-40	mA
TTL Input Voltage	V_{LOW} V_{HIGH}	Logic 0 Logic 1	0 2		0.8 5.0	V
Low Level Output Voltage Output A, B or C	V_{OUTL}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, Source current from $+V_{CC}$=50mA	$+V_{CC}$ -1	$+V_{CC}$ -0.5	$+V_{CC}$ -0.1	V
Low Level Output Voltage Output A, B or C	V_{OUTH}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, Sink current from $-V_{EE}$= 50mA	$-V_{EE}$ +1	$-V_{EE}$ +0.5	$-V_{EE}$ -1	V
Switching Time	T_{SW}	$+V_{CC}$=5V, $-V_{EE}$=-15V to -200V, F =10kHz, 50% TTL to 10% or 90% RF output voltage		1.5	2	usec

RFD3T5N200-703 Pin Out





Pin Out Description

Pin	Pin Name	Input/Output	Description
1	CTL1	I	TTL input control (CTL1)
2	$+V_{CC}$	I	+5V supply voltage input
3	$-V_{EE}$	I	Negative high voltage (-15 to -200V) input
4	CTL2	I	TTL input control 2 (CTL2)
5	CTL3	I	TTL input control 3 (CTL3)
6	GND		$+V_{CC}$ & $-V_{EE}$ ground return
7	GND		$+V_{CC}$ & $-V_{EE}$ ground return
8	GND		$+V_{CC}$ & $-V_{EE}$ ground return
9	Output C	O	Bias voltage/current output from driver port C
10	Output B	O	Bias voltage/current output from driver port B
11	Output A	O	Bias voltage/current output from driver port A
12	GND		$+V_{CC}$ & $-V_{EE}$ ground return
13	GND		$+V_{CC}$ & $-V_{EE}$ ground return
14	GND		$+V_{CC}$ & $-V_{EE}$ ground return
15	GND		$+V_{CC}$ & $-V_{EE}$ ground return
16	GND		$+V_{CC}$ & $-V_{EE}$ ground return

Truth Table

CTL1 (notes 1 & 2)	CTL2 (notes 1 & 2)	CTL3 (notes 1 & 2)	Driver Output Section A	Driver Output Section B	Driver Output Section C
V_{HIGH}	V_{LOW}	V_{LOW}	V_{OUT}=+V_{CC} V, current sourcing mode	V_{OUT} ~ -V_{EE} V, Current sinking mode	V_{OUT} ~ -V_{EE} V, Current sinking mode
V_{LOW}	V_{HIGH}	V_{HIGH}	V_{OUT} ~ -V_{EE} V, Current sinking mode	V_{OUT}=+V_{CC} V, current sourcing mode	V_{OUT}=+V_{CC} V, current sourcing mode
V_{HIGH}	V_{LOW}	V_{HIGH}	V_{OUT}=+V_{CC} V, current sourcing mode	V_{OUT} ~ -V_{EE} V, Current sinking mode	V_{OUT}=+V_{CC} V, current sourcing mode
V_{LOW}	V_{HIGH}	V_{LOW}	V_{OUT} ~ -V_{EE} V, Current sinking mode	V_{OUT}=+V_{CC} V, current sourcing mode	V_{OUT} ~ -V_{EE} V, Current sinking mode
V_{HIGH}	V_{HIGH}	V_{LOW}	V_{OUT}=+V_{CC} V, current sourcing mode	V_{OUT}=+V_{CC} V, current sourcing mode	V_{OUT} ~ -V_{EE} V, Current sinking mode
V_{LOW}	V_{LOW}	V_{HIGH}	V_{OUT} ~ -V_{EE} V, Current sinking mode	V_{OUT} ~ -V_{EE} V, Current sinking mode	V_{OUT}=+V_{CC} V, current sourcing mode
V_{LOW}	V_{LOW}	V_{LOW}	Note 3	Note 3	Note 3
V_{HIGH}	V_{HIGH}	V_{HIGH}	Note 3	Note 3	Note 3

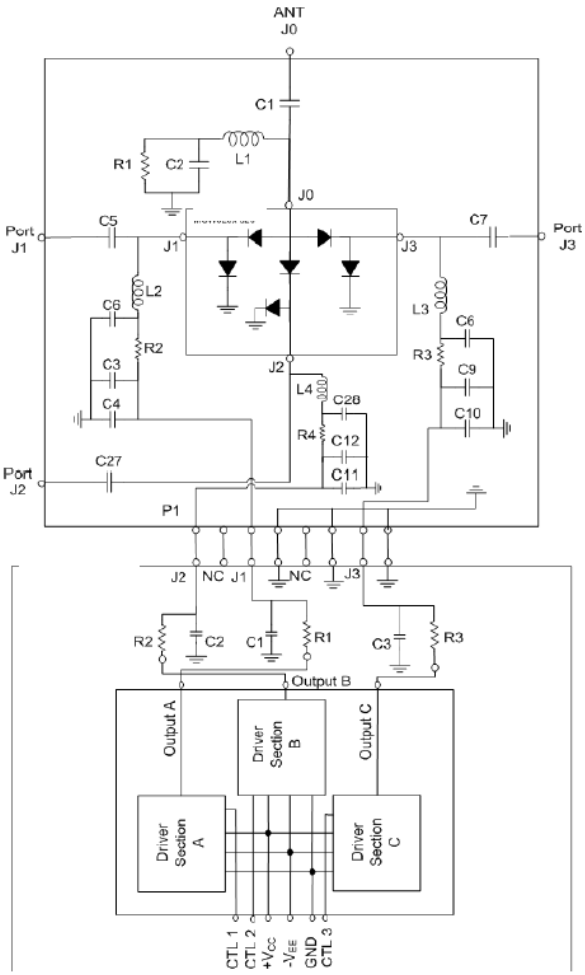
Notes:

1) 2V ≤ VHIGH ≤ 5V
2) 0V ≤ VLOW ≤ 0.8V
3) Not recommended state

Control of Symmetrical SP3T Switch

The RFD3T5N200-703 can control a symmetrical SP3T series-shunt PIN Diode switch. Each driver section is connected to one series-shunt switch element to provide biasing voltages required in the two operating states: RF State 1 and 0. The RF State of the SP3T is determined by the inputs to the three Control signals: CTL1, CTL2 & CTL3. Each Control signal states drives the SP3T into a state where one port is in the Low Loss state while the other two ports are in the Isolation state.

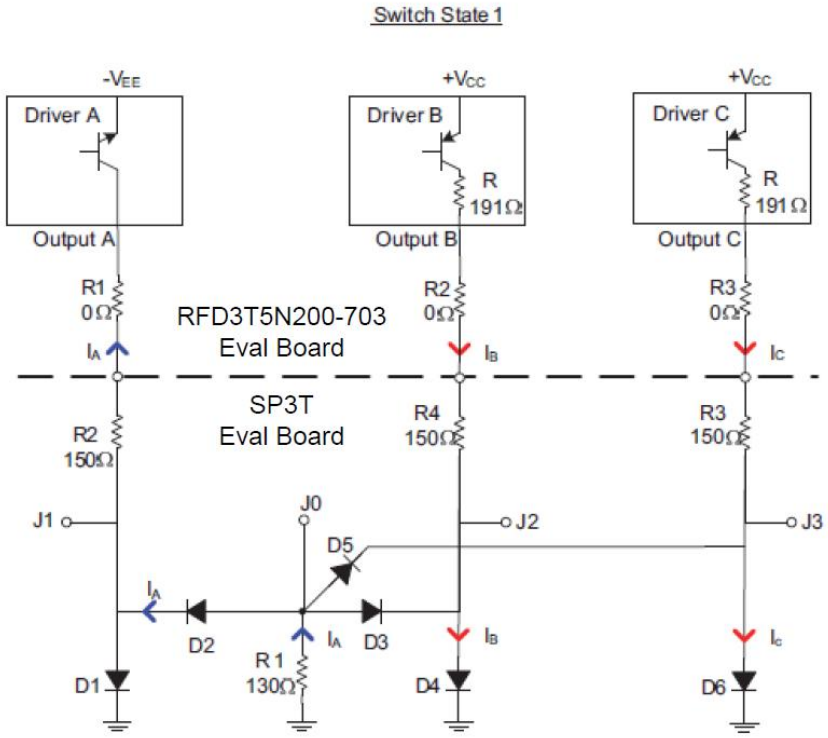
CTL1	CTL2	CTL3	RF State	Path J0 to J1	Path J0 to J2	Path J0 to J3	Output A J1 Bias	Output B J2 Bias	Output C J3 Bias
LOW	HIGH	HIGH	1	Low Loss	High Isolation	High Isolation	V_{OUT} ~ $-V_{EE}$, Current sink mode	V_{OUT}~$(+V_{CC} - I_{OUT} \times 191)$V, current source mode	V_{OUT}~$(+V_{CC} - I_{OUT} \times 191)$V, current source mode
HIGH	LOW	HIGH	2	High Isolation	Low Loss	High Isolation	V_{OUT}~$(+V_{CC} - I_{OUT} \times 191)$V, current source mode	V_{OUT} ~ $-V_{EE}$, Current sink mode	V_{OUT}~$(+V_{CC} - I_{OUT} \times 191)$V, current source mode
HIGH	HIGH	LOW	3	High Isolation	High Isolation	Low Loss	V_{OUT}~$(+V_{CC} - I_{OUT} \times 191)$V, current source mode	V_{OUT}~$(+V_{CC} - I_{OUT} \times 191)$V, current source mode	V_{OUT} ~ $-V_{EE}$, Current sink mode



Positive & Negative Voltage PIN Diode Switch Driver

RF State 1

The schematic shown below reflect RF State 1 for the RFD3T5N200-703 driver interconnected to a SP3T evaluation board.



In RF State 1, the voltage from Output A of Driver A is approximately equal to $-V_{EE}$ supply voltage. This provides a forward bias to the series PIN diode, D2, between the J0 and J1 ports. The magnitude of the resultant bias current through D2 is primarily determined by the output voltage from Output A, the magnitude of the forward voltage across D2 and the sum of the resistance of R1 and R2 on the SP3T evaluation board and R1 on the driver evaluation board. This current is nominally -100 mA.

At the same time, the PIN diodes D4, D6 connected between J2 and ground, J3 and ground are also forward biased by the voltage produced at Output B of Driver B, Output C of Driver C. The voltages are slightly less than $+V_{CC}$ due to the voltage drop across the 191Ω internal resistors. Under this condition, the PIN diodes, D3, D5 connected between the J0, J2 and J0, J3 ports are reverse biased. The magnitude of the bias currents through D4 is primarily determined by $+V_{CC}$, the magnitude of the forward voltage across D4 and the sum of the resistanceof R4 on the switch eval board, R2 on the driver eval board and the 191Ω internal resistor. Similarly, the bias currents through D6 is determined by $+V_{CC}$, the magnitude of the forward voltage across D6 and the sum of the resistances of R3 on the switch eval board, R3 on the driver eval board and the 191Ω internal resistor. Nominally current through each shunt diode D4 and D6 is 15mA.

The series PIN diodes, D3, D5 must be reverse biased during RF State 1. The reverse bias voltage must be sufficiently large to maintain this diode in its non-conducting, high impedance state when a large RF signal voltage may be present in the J0 to J1 path. The reverse voltage across D3 is the arithmetic difference of the

potentials at its anode and cathode, similarly reverse voltage across D5 is the arithmetic of the potentials at its anode and cathode.

The potential at D3's cathode is equal to the forward voltage of D4 and the potential at D5's cathode is equal to the forward voltage of D6. These voltages are nominally 0.8V. The potential at D3's anode is equal to the voltage drop across R1 of the SP3T eval board. This voltage is the product of the current through D2 and the resistance of R1. The voltage across D3 is given by:

$$V_{D3} = V_{ANODE\ D3} - V_{CATHODE\ D3} = V_{ANODE\ D3} - 0.8$$

$$V_{ANODE\ D3} = I_A \times R1 = [(-V_{EE} + VD2)/(R1 + R2)] \times R1 \sim [(-28 + 0.8)/280] \times 130 = -12.6V$$

$$V_{D3} = V_{ANODE\ D3} – V_{CATHODE\ D3} = -12.6 – 0.8 = -13.4V$$

The potential at D5 anode can also be calculated as above. The anode of D5 potential will be equal to the potential of the anode of D3.

The minimum voltage required to keep D3 and D5 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the D3 and D5 anodes, the frequency of the RF signal and the characteristics of the seriesdiode, among other factors. The minimum required voltage can be calculated as described in the section "Minimum Reverse Bias Voltage".

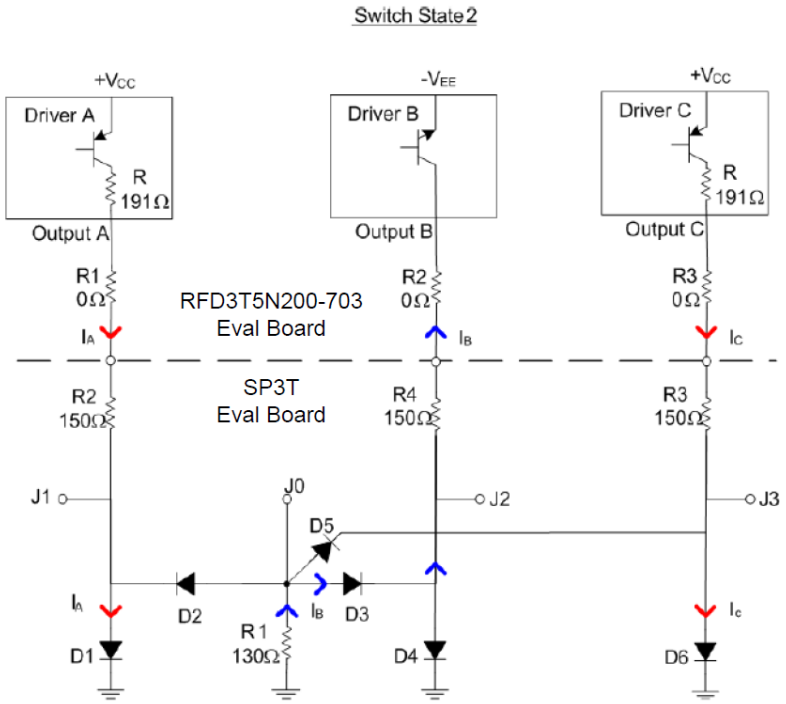
RF State 2

The simplified DC Bias circuit schematic for RF State 2 for the RFD3T5N200-703 driver interconnect to the SP3T eval board is shown below.

In RF State 2, the voltage from Output B of Driver B is approximately equal to the $–V_{EE}$ supply voltage. This provides a forward bias to the series PIN diode, D3, between the J0 and J2 ports. The magnitude of the resultant bias current through D3 is primarily determined by the output voltage from Output B, the magnitude of the forward voltage across D3 and the sum of the resistances of R1 and R4 on the SP3T eval board and R2 on the driver eval board. Under this condition, the series diodes D2 and D5 are reversed biased.

The magnitude of the bias current through D1 is primarily determined by $+V_{CC}$, the magnitude of the forward voltage across D1 and the sum of the resistances of R2 on the switch eval board, R1 on the driver eval board and the internal 191Ω resistor. Similarly, the magnitude of the bias current through D6 is primarily determined by +VCC, the magnitude of the forward voltage across D6 and the sum of the resistances of R3 on the switch eval board, R3 on the driver eval board and the internal 191Ω resistor. The nominal currents through each of these shunt diodes is 15mA.

The series PIN diodes, D2 and D5 must be reversed biased during RF State 2. The reverse bias voltage must be sufficiently large to maintain this diode in its non-conducting, high impedance state when a large RF signal voltage may be present in the J0 to J2 path. The reverse voltage across D2 and the diode D5 is the arithmetic difference of the potentials at their anode and cathode terminals.



The potential at D2's cathode is equal to the forward voltage of D1 and the potential at D5's cathode is equal to the forward voltage of D6. This voltage is nominally 0.8V. The potential at D2's anode is equal to the voltage drop across R1 of the SP3T eval board. The voltage is the product of the current through D3 and the resistance of R1. The voltage across D2 is given by the following:

$$V_{D2} = V_{ANODE\ D2} - V_{CATHODE\ D3} = V_{ANODE\ D2} - 0.8$$

$$V_{ANODE\ D2} = I_B \times R1 = [(-V_{EE} + V_{D3})/(R1 + R2)] \times R1 \sim [(-28 + 0.8)/280] \times 130 = -12.6V$$

$$V_{D2} = V_{ANODE\ D2} - V_{CATHODE\ D2} = -12.6 - 0.8 = -13.4V$$

Similarly, the voltage across D5 can be calculated and the value would be equal to -13.4V.

The minimum voltage required to keep the diodes D2 & D5 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at anodes of D2 and D5, the frequency of the RF signal and the characteristics of the series diodes, among other factors. The minimum required voltage can be calculated as described in the section "Minimum Reverse Bias Voltage".

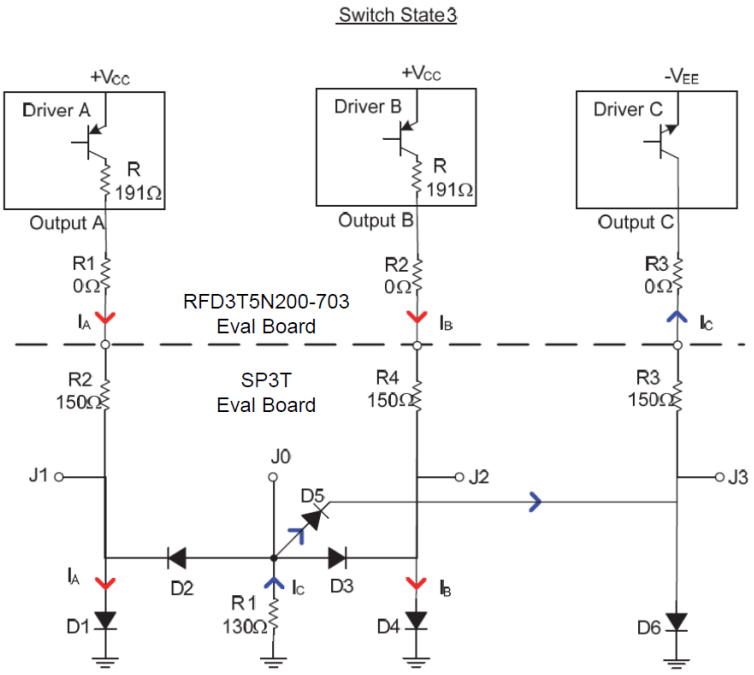
RF State 3

The simplified DC bias circuit schematic for RF State 3 for the RFD3T5N200-703 driver interconnected to the SP3T eval board is shown below.

In RF State 3, the voltage from Output C of Driver C is approximately equal to the $-V_{EE}$ supply voltage. This provides a forward bias to the series PIN diodes, D5, between the J0 to J3 ports. The magnitude of the resultant bias current through D5 is primarily determined by the output voltage from Output C, the magnitude of the forward voltage across D5 and the sum of the resistances of R1 and R3 on the SP3T eval board and R2 on the driver eval board. This current is nominally -100mA.

At the same time, the PIN diodes, D1 and D4 connected between J1, ground and J2 and ground are also forward biased by the voltage produced at output A of Driver A, Output B of Driver B respectively. The driver output voltages are a bit less than $+V_{CC}$ due to the voltage drop across the 191Ω internal resistor. Under this condition the series diodes D2 and D5 are both reversed biased.

The magnitude of the bias current through D1 is primarily determined by $+V_{CC}$, the magnitude of the forward voltage across D1 and the sum of the resistance of R2 on the switch eval board, R1 on the driver eval board and the internal 191Ω resistor. Similarly, the magnitude of the bias current through D4 is determined by $+V_{CC}$, the magnitude of the forward voltage across D4 and the sum of the resistances of R4 on the SP3T eval board, R2 on the driver eval board and the internal 191Ω resistor. The nominal currents through each of these shunt diodes is 15mA.



The series PIN didoes, D2 and D3 must be reversed biased during RF State 3. The reverse bias voltage must be sufficiently large to maintain this diode in its non-conducting, high impedance state when a large RF signal voltage may be present in the J0 to J3 path. The reverse voltage across D2 and the diode D3 is the arithmetic difference of the potentials at their anode and cathode terminals. The potential at D2's cathode is equal to the voltage of D1 and the potential at D3's cathode is equal to the forward voltage of D4. The voltage is nominally 0.8V.

The potential at D2's anode is equal to the voltage drop across R1 of the SP3T eval board. This voltage is the product of the current through D3 and the resistance of R1. The voltage across D2 is determined by the following:

$$V_{D2} = V_{ANODE\ D2} - V_{CATHODE\ D3} = V_{ANODE\ D2} - 0.8$$

$$V_{ANODE\ D2} = I_B \times R1 = [(-V_{EE} + V_{D3})/(R1 + R2)] \times R1 \sim [(-28 + 0.8)/280] \times 130 = -12.6V$$

$$V_{D2} = V_{ANODE\ D2} – V_{CATHODE\ D2} = -12.6 – 0.8 = -13.4V$$

Similarly, the voltage across the D3 can be calculated, and the value would beequal to -13.4V.

The minimum voltage required to keep the diodes D2 and D3 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the anode terminals of diodes D2 and D3, the frequency of the RF signal and the characteristic of the series diode, among other factors. The minimum required voltage can be calculated as described in the section “Minimum Reverse Bias Voltage”.

Calculation of Resistor Values

The magnitude of the forward bias current applied to the series diode is set by the magnitude of the supply voltage –VEE, which is nominally 28V, the value of resistors R1 and R2 or R3 on the SP3T eval board as well as R1 on the driver eval board, the forward of the series diode, VDIODE, among other factors. Given the desired currentvalue, the resistance is given by the following formula:

$R_{TOTAL} = R_{1 \text{ or } 2(\text{driver board})} + R_{2 \text{ or } 3 (\text{SP3T eval board})} + 191\Omega = (+V_{CC} - V_{DIODE})/ I_{BIAS}$

Minimum Reverse Bias Voltage

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1 + \left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1 + \sqrt{1 + \left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal given by the following variables:

$|V_{DC}|$ = magnitude of the minimum DC reverse bias voltage

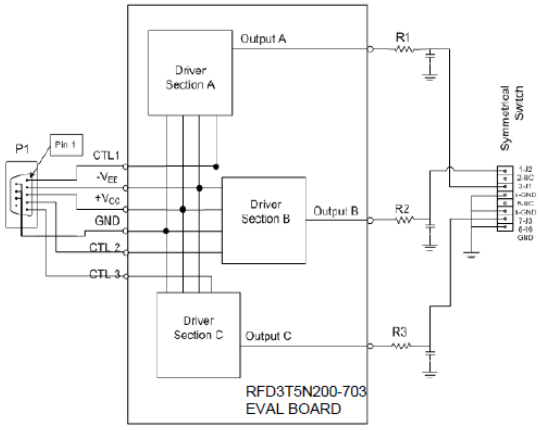
$|V_{RF}|$ = magnitude of the peak RF voltage(including the effects of VSWR)

f_{MHz} = lowest RF signal frequency expressed in MHz

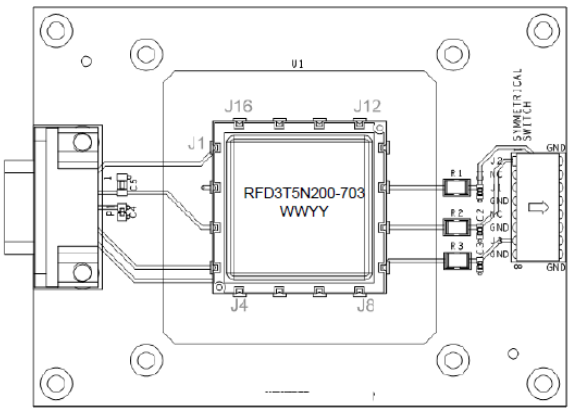
D = duty factor of the RF signal

W_{mils} = I region thickness of the PIN Diode (expressed in mils)

RFD3T5N200-703
EVAL BOARD



RFD3T5N200-703
EVAL BOARD LAYOUT



The RFD3T5N200-703 eval board contains several passive components. R1 and C1 are optional components which may be used to shape the output signal of Output A. Likewise, R2 and C2, R3 and C3 may be used to shape the output signal from Output B, Output C respectively. C1, C2 and C3 capacitors are normally not installed. R1, R2 and R3 are installed with 0Ω, 0.5W resistors. The positive supply voltage, nominally 5V, is designated as $+V_{CC}$. The negative supply voltage, nominally -15V to -200V, is designated as $-V_{EE}$.

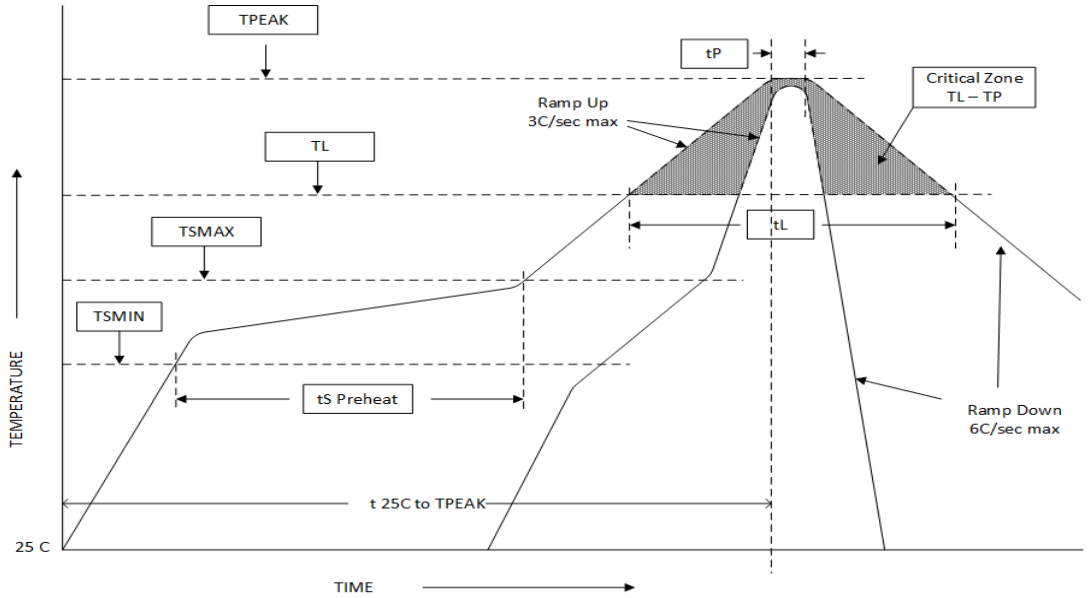
There are two multi-pin connectors on the board. P1 is a DB-9 male connector which facilitates connection of the TTL control signal, supply voltages and ground to the eval board. Symmetrical switch is a 16 pin female header which can be used to connect directly to the male header on the symmetrical SP3T Eval Board. The pin out for these connectors are shown below:

Assembly Instructions

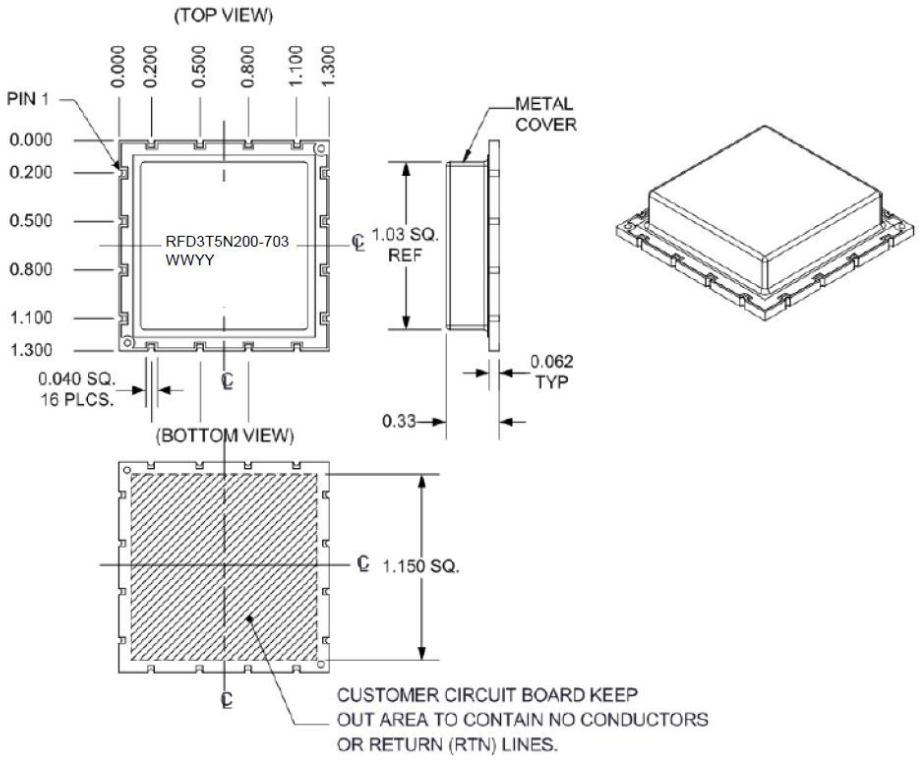
The RFD3T5N200-703 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 180 sec
T_{smax} to T_L Ramp up Rate	 	 3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFD3T5N200-703 Package Outline Drawing



Notes:

1) Circuit Board material is FR4.
2) Metallization: 2 0z Cu followed by 150uin (TYP), followed by 4uin (TYP) Au
3) Unit = inches

Part Number Ordering Detail:

The RFD3T5N200-703 PIN Switch Driver is available in the following format:

Part Number	Description	Packaging
RFD3T5N200-703	SP3T Positive & Negative Voltage Switch Driver	Tube
RFD3T5N200-703-EVB	RFD3T5N200-703 Evaluation Board	Box